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Design of High-Performance Pipeline Analog-to-Digital Converters in Low-Voltage Processes

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ABSTRACT: This research presents a high-resolution Pipeline ADC in low-voltage processes. The removal of the Sample-and-Hold circuit greatly reduces the power consumption and area use of the Pipeline ADC. A rail-to-rail input is achievable with the sample-and-hold stage removed from the system. This increases the available signal range, thereby improving the SNR of the system. A final ADC structure incorporating two reference voltages was perused and a calibration scheme for correcting reference mismatch errors was developed. The optimization greatly improved the noise and area performance in the design. The design implementation portion of the paper covered many important parts in the design of a high-resolution ADC Pipeline stage. The result shows that our approach can outperform previous methods.

***Keywords*:** High-Performance Pipeline, Analog-to-Digital, Converters, Low-Voltage Processes.

INTRODUCTION

High-performance applications such as broadband communication systems require high-performance analog-to-digital converters (ADCs) with high-resolution and band-width (over 14 bits and several MHz). Such applications are often the domain of pipeline ADCs, due to their highly efficient and conversion-speed-centric architecture. The in-creasing focus on low-voltage digital processes places great strains on the design of such systems and makes them very costly to implement using current pipeline ADC design techniques (Siragusa and Galton, 2004, Hadidi 1990, Temes, 1992). This paper explores these issues in detail and presents alternative design techniques for economically achieving these performance goals in modern low-voltage processes (Chang, 2009).

Analog-to-digital converters are important components in applications requiring the interface between analog and digital domains. These are varied and numerous and range from digital radio systems to military and medical sensors to wire-line and wireless communications.

There are a number of different ADC architectures available to accomplish the data conversion task; however, no single architecture is independently suited for all applications. As illustrated in Fig. 1, these architectures span a range of intended resolutions and conversion speeds. Some also have differences in power-consumption and conversion latency and must be chosen to fit the given application

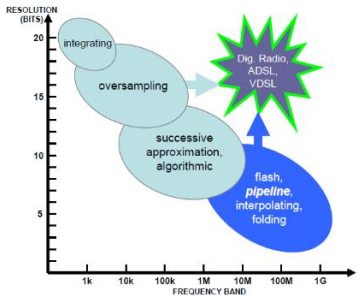

Figure 1. Types of analog-to-digital converters

Consumer acceptance and use of digital communication technology coupled with advancements in the technology of wired and wireless communications have increased the demand for high-performance ADCs that must be incorporated in these systems.

One example of this trend is the rising speed requirements for DSL systems. Digital subscriber lines (DSL) target unused bandwidth in current twisted-pair telephone infrastructure. These lines were originally used to carry only low-bandwidth voice data and therefore leave a large portion of the overall bandwidth unused. This unused bandwidth is utilized by DSL for high-speed digital communications. Current standards for Asymmetric DSL (ADSL) and Very high-speed DSL (VDSL) require ADCs used in these systems to meet conversion requirements of 2.5 MS/s and 24 MS/s respectively with resolutions on the order of 13 to 14 bits [1]. These requirements will only increase as the technology matures and as consumers demand more bandwidth for applications such as video streaming.

The requirements imposed by this application (and many others) have spawned research in two major areas, represented by the arrows in Fig. 1. One research direction concerns itself with the improvement of Nyquist-rate ADCs. Pipeline ADCs are currently the most researched of these type of ADCs. Their architecture is most suited for medium resolution and high speed, and therefore requires accuracy improvements to meet the stringent digital communication system requirements. Recent work in current analog processes has shown effective resolutions of 12 bits while previous designs in older analog processes have shown effective resolutions of 13 bits.

The other research direction concerns itself with the improvement of oversampling ADCs. These ADCs are often utilized for high to very-high resolution and low to medium speed. The high resolution is achieved by oversampling, which trades bandwidth for resolution by averaging multiple samples. Further improvement can be attained by use of z-domain functions aimed at shaping the noise of the ADC. Recent work done in this area focuses on improving the speed of these ADCs.

This paper covers the first research direction listed and includes other important considerations for designing in today's modern semiconductor processes. At the same time as communications applications are seeing increased system performance requirements, digital CMOS processes are following a trend of reduced supply voltages. This is motivated by speed improvements and area savings achievable with smaller device dimensions (Liu et al., 2004). For many analog applications, a lower supply voltage is a crippling design limitation this is especially true for ADC designs whose accuracy directly depends on the power of the input signal. Many new processes are developed with processing options that allow the use of high-voltage analog devices, but these make the cost of manufacturing mixed-signal and SOC (System on Chip) microchips much more expensive (Nair and Harjani, 2004).

The challenge from this design perspective is to achieve high accuracy in an ADC using modern low-voltage digital transistors. This paper focuses on improving the accuracy of pipeline ADCs while mitigating manufacturing costs as much as possible.

There are two main design concepts presented in this paper. The first is based on published work by Mercer (1996) and work by Chiu et al., (2004). The second is based on low-voltage ADC design concepts developed by Jipeng Li while he was a Ph.D. student at Oregon State University. The design concepts are:

Removal of sample-and-hold (S/H): The removal of this key block provides significant noise and power savings for pipeline ADCs; however, it places extra strain on the first stage of a pipeline ADC. This stage now must take care of the sampling function and must do so on two independent signal paths.

Rail-to-rail input: Signal power is greatly increased by allowing a rail-to-rail input. The active pipeline stages cannot drive this level at their outputs and therefore the inter-pipeline stage residue signal amplitude must be reduced. This is compensated for with system design changes that may introduce a gain error in the pipeline ADC (Silva, 2012). A calibration scheme is developed to combat this error source.

Other contributions of this work include discussion on multi-bit stage optimization, stage scaling, and high-gain, wide-swing opamp design. The overall contributions culminate in the presentation of a design strategy for achieving high performance in pipeline ADCs suitable for today's and tomorrow's high-bandwidth communication technologies.

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MATERIALS AND METHODS

This section will cover system design considerations for high-resolution, medium-speed Pipeline ADCs. Specifically, 14-bits of ENOB at 20 MSPS (Mega-Samples Per-Second) is the desired performance of the Pipeline ADC. The high-resolution requirement places stringent requirements on the front-end of the pipeline and therefore substantial thought and consideration should be placed in choosing the system structure. A poor choice in architecture can lead to excessive waste in power and area. (Balmelli and Huang, 2012).

Additionally, the noise contributed from kT/C sampled thermal noise dictates that for each single-bit increase in SNR, a 4x increase in sampling capacitance is required.

As mentioned in the introduction, recent designs have limited their ENOB to approximately 12-bits. The 2-bit improvement desired for this work requires a 16x increase in capacitance to improve the SNR performance of similar converters to the required level (Mehr and Singer, 2000). Achieving SNR improvement economically will require some extra effort in the system level design.

2.1. Bits-Per-Stage Architecture

One major architecture consideration in the design of any Pipeline ADC is the choice of bits resolved per-stage. Low resolutions per-stage are generally suited for lower resolution and higher speed Pipeline ADCs, while high resolutions per-stage (of-ten referred to as multi-bit) are more suited to the high accuracy requirements of the applications mentioned in this paper.

There are three major metrics within MDAC design that can determine the required cost (in power and area) dependant on per-stage-resolution. They are conversion speed, converter accuracy, and noise, and are assumed to be fixed design requirements.

A simplified MDAC structure is shown in Figure 2 for reference during this discussion.

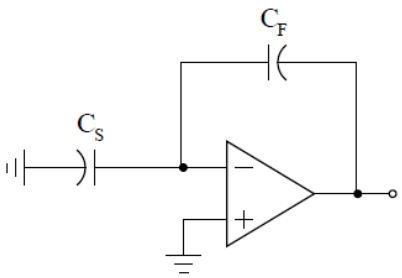

Figure 2. Simple MDAC Reference (Amplification Phase)

Conversion speed is directly related the per-stage-resolution by way of the loop feedback factor. The feedback factor is easily determined to be

$$\beta = \frac{C_F}{C_S + C_F},$$

where CS and CF are the capacitance values as shown in Fig. 2. Stage gain (determined by per-stage resolution) is equal to CS/CF , and by substitution, the feedback factor becomes

$$\beta = \frac{1}{G+1},$$

A common starting design parameter is the loop unity-gain and width (UGBW). This determines (in conjunction with capacitive loads and feedback factor) such design parameters as opamp power consumption and device sizes, and is stipulated by stage settling requirements. Loop UGBW relates to the feedback factor (fi) in equation 3.2 by the following equation:

$$\omega_{t(open)} = \omega_{t(loop)} \frac{1}{\beta} = \omega_{t(loop)}(G+1),$$

where wt(open) is the required amplifier open-loop UGBW to meet the loop UGBW requirement. Above Equation (3.3) shows that increasing the stage gain increases the bandwidth requirement, and therefore the power consumption of the MDAC stage; however there is a compensating factor. The gain increase reduces the number of stages required to meet the design goal, but at a diminishing rate in comparison to power consumed. Increasing the stage-resolution increases the power consumption needed to meet the settling requirements (Putter, 2011).

These statements ignore the common practice of load-scaling from stage-to-stage, which would improve the power consumption required for setting. The incorporation of this scaling can actually improve the power consumption required for settling; however, this breaks-down as the desired A/D conversion speed approaches the given

technology's ft limitations. In this condition, there is a diminishing return on open-loop UGBW for increased power consumption. This is why single-bit-per-stage Pipeline ADCs (or 1.5 bit-per-stage) are common for high-speed data conversion systems.

Converter Accuracy Overall converter accuracy sets limitations on allowable error in the analog signal between stages in the pipeline. For instance, if an overall converter accuracy (noise and linearity) requirement is 12 bits, the sample-and-hold stage must be able to output a greater-than 12 bit accurate analog output signal for the following stage.

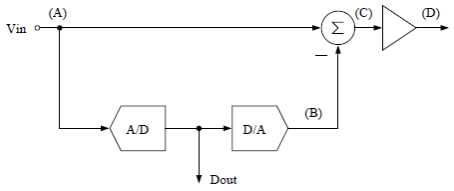

Figure 3. System-Level Pipeline ADC Stage

A system-level representation of a Pipeline ADC stage is shown in Fig. 3; it can be seen that the signal accuracy at points (B) and (C) must match the accuracy at point (A). After the gain, point (D) need only be as accurate as point (A) divided by the gain. This implies that the output accuracy requirement is lessened when more bits are resolved within a given pipeline stage.

Sampled Noise

High accuracy ADC designs require careful consideration of noise contributors and system architecture to realize power efficient ADCs while still maintaining desired accuracy levels. Again, the simple MDAC example in Fig. 2 is used to develop an equation illustrating the effect of stage-resolution on this design parameter.

The charge noise of each capacitor is given as $\bar{q}_n^2 = kTC$. The output referred voltage noise is then

$$\overline{v}_{n(out)}^2 = \frac{2kTC_S + 2kTC_F}{C_F^2},$$

where it is assumed that each capacitor samples a value during each of two phases (generating the `2' in `2kTC'). Reduction of the equation provides

$$\overline{v}_{n(out)}^2 = \frac{2kT}{\beta C_F} = \frac{2kT}{C_F}(G+1)$$

Referring above to the input of the MDAC give

$$\overline{v}_{n(in)}^2 = \frac{2kT}{C_F}\left(\frac{G+1}{G^2}\right)$$

A simple substitution from the MDAC gain equation, G = CS/CF , gives

$$\overline{v}_{n(in)}^2 = \frac{2kT}{C_S}\left(\frac{G(G+1)}{G^2}\right) = \frac{2kT}{C_S}\left(\frac{G+1}{G}\right)$$

Actual MDAC implementations would use the feedback capacitor CF for sampling as well { this reduces the G+1 term to G. Above Equation then shows that sampled, input referred noise has no dependance on per-stage resolution. Active circuit noise can be considered in a similar fashion. Figure 4 is used to develop the equation describing active circuit dependance on per-stage resolution. There are two noise sources shown in the figure; each source will be considered independently by way of superposition.

2-2-Number of Stages and Noise

Another important stage resolution dependant noise consideration is the more stages vs. less stages tradeoff. This is essentially the same as less resolution per-stage vs. more resolution per-stage, but will be considered on a more basic architectural level.

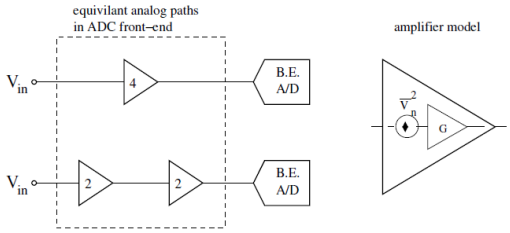

Figure 4. Stage Number Noise Tradeoff Comparison

A simple comparison of two stage conversion size options is shown in Fig. 4. Both signal paths achieve the same signal conversion before the back-end A/D and both stages have the same overall gain from the input to the back-end A/D. If it is assumed all amplifiers have the same input referred noise, as implied it is easy to see that the single-amplification signal path has less noise than the other path. This makes intuitive sense because more stages means more devices and more opportunity for noise to be injected into the signal path.

2-3- Sample-and-Hold Removal

One major contributor to overall system noise and power consumption is the Sample-and-Hold (S/H) circuit. The circuit provides a sampled, unity-gain signal to the first pipeline stage, which allows some flexibility in the operation of the pipeline stage. The sampling function can, however, be incorporated into the first stage of the pipeline if the Sample-and-Hold is removed. The removal of the S/H will effectively cut the required power consumption *and* capacitor area in half. This is because the unity-gain provided by the S/H circuit implies equal relative noise contributions between the S/H and the first Pipeline stage. For high-resolution designs, the noise contributions of these stages are usually dominated by kT/C thermal noise. If it is assumed that pipeline stages after the first stage consume a minimal amount of power and area in the overall system budget, then the power and area savings from the S/H removal is approximately half.

2-4-Rail-to-Rail Input

The removal of the sample-and-hold circuit saves a lot of power and makes meeting the ENOB goal presented at the beginning of this section more approachable. Now that the S/H is no longer present in the signal path, the input voltage is no longer limited to the linear output range of an active stage. In fact, the only limitation on the signal is process voltage limitations commonly the power supply voltages. The implementation of a true rail-to-rail (RTR) input is now possible.

This signal range is a great boost for economically achievable signal-to-noise ratio, and therefore will also help reach the ENOB goals presented in this paper.

This new input signal range requires a change in the first pipeline stage. The comparators must compare over the input signal range which is now the power supply, and the DAC portion of the MDAC must inject references equal to the supply rails during the amplification phase. This is equivalent to changing the stage reference voltage to be equal to the supply rails. The operation of the pipeline stage, with this change, is now the same as the classical pipeline stage.

Classical pipeline stages require that the MDAC's active output stage drive signals to the reference voltage. For the architecture presented, this implies driving the output to the power supply rails (*VREF*2 for later reference). The amplifier responsible for creating the output level is not capable of driving to the supply rails accurately.

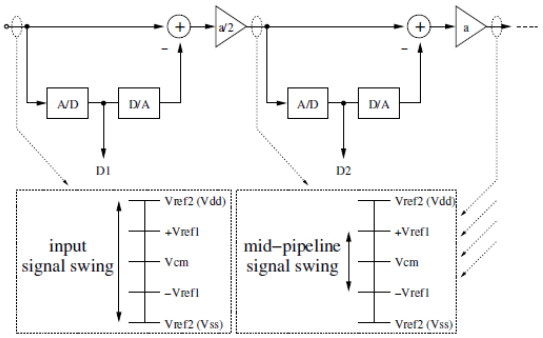

Figure 5. Two-Reference Pipeline Architecture

The final architecture is shown in Figure 5.

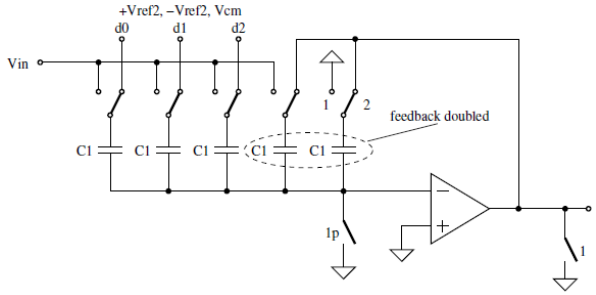

Figure 6. First Stage MDAC Redesign for Two-Reference Pipeline

The circuit implementation of this MDAC is very straightforward; the only change required is that the feedback capacitance must be doubled (Fig. 6). The reduced gain increases the contribution of noise from following stages, but as long as the stage resolution of the first stage is chosen to be large enough (more than 1.5 bits-per-stage), the first stage will still provide some help. One beneficial result of this architecture decision is that the feedback factor is increased, and therefore the required power consumption of the MDAC stage will be reduced.

An issue with this two-reference solution is the potential mismatch between the two references. If the references are not exactly 2x from each other, then there will be some gain error injected at the boundary between the two references. This will introduce a non-linear error in the overall conversion. A method for correcting this error will be discussed shortly.

The decision of what architecture to use in a given Pipeline ADC design ultimately becomes an optimization problem. The variable quantities are per-stage resolution and inter-stage power and capacitor scaling. The constraint for this optimization is a defined noise performance, and the costs to be minimized are total area and power consumption.

A basic optimization method for Pipeline ADC power was introduced by Erdogan (1999) wherein two different levels of optimization are discussed (zeroth order and first order).

The basis of this optimization is to vary a taper factor that determines the rate at which the sampling capacitors are scaled down the pipeline in a Pipeline ADC. This was done for several per-stage resolutions.

The zeroth order optimization assumes that the load capacitance is dominated by the sampling capacitance of the current stage. This ignores the effect of feedback factor and loading of the following stage. The power is then assumed to be directly proportional to the load capacitance. The first-order optimization takes into consideration both the feedback factor and the following stage's load capacitance when computing the total load. As in the zeroth-order optimization, the power is assumed to be directly proportional to the load capacitance.

1-Implementation and discussion

In the previous section system architecture was chosen. This decision was based on various power and area optimization considerations. The final result was a two- reference Pipeline ADC with 3.5 bits per-stage.

The first stage is the most important stage in the design. The remaining stages see the input after it has experienced a fair amount of gain and after some of the signal has already been resolved; therefore, the requirements on the back-end stages will be much lower than the first stage's requirements. Some of the specifications that the

first stage must meet are: low-noise>15 bits linearity sampling, >12 bits linearity at the output, >14 bit settling during sampling, and >11 bit settling on the output. The sampled, thermal noise portion of the overall noise has already been accounted for with the optimization in the previous section. The linearity is a function of the linearity of the components and open-loop amplifier gain. Settling time is determined by the pole locations within the circuits and can be determined by RC-networks as well as opamp bandwidth and stability.

3-1- First Stage Sampling

The matching of both sampling paths is discussed in detail; however, the linearity requirements of the input sampling were not discussed. Furthermore, the impact of rail-to-rail input on the input sampling circuits was not covered. The linearity requirements of the sampling circuit are determined by the overall desired linearity. The first stage sampling linearity must therefore be better than the overall desired linearity. For a 14-bit ENOB Pipeline ADC it is desirable that the linearity be at least 15 bits. This allows the noise component of the ENOB measurement to be dominant. Additionally, if the linearity requirement is met for the entire system, then the DNL and INL should also be at least 15 bits.

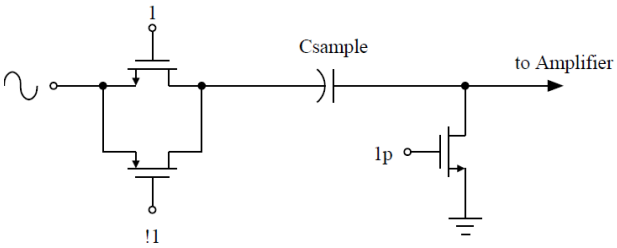

Figure 7. Input Sampling with CMOS Switch

A common implementation of a switched-capacitor input sampling circuit is shown in Figure 7. The floating" CMOS switch (or transmission gate) passes signals anywhere in the range from the positive power supply to the negative power supply.

3-2-Bootstrapping

The sampling linearity can be greatly improved if the gate-source voltage is held constant for all input signals. A simple example of this would be to place a voltage source between the input (source) and gate of an NMOS switch. Ideal voltage sources are generally not within an IC design, therefore capacitors are often used as a replacement for the voltage source. A sampling system incorporating a simplistic version of bootstrapping is shown in Figure 8.

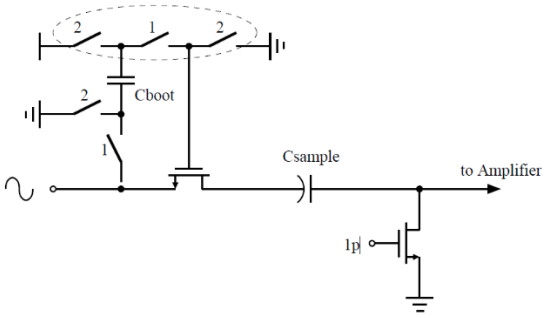

Figure 8. Input Sampling with Bootstrapped NMOS Switch

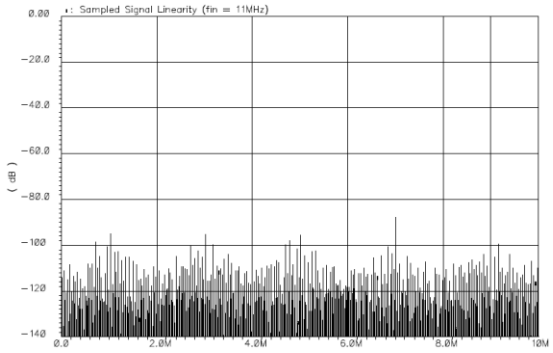

Figure 9. Bootstrapped NMOS Switch Sampling Linearity

One of the major dificulties with bootstrapping clock circuits is keeping all transistors from experiencing voltages greater than the power supply. For example, the switches on the gate of the NMOS switch (circled) would experience source-bulk and drain-source voltages greater than the power supply. A popular circuit used to circumvent this problem was introduced by Dessouky and is used in this work as well. Linearities of about 15 bits can be achieved in the available 0.18um CMOS process with a bootstrapped NMOS switch. (Fig. 9).

3-3- Final MDAC System

The final MDAC implementation is shown in Figure 10. The input is differentially sampled on sixteen unit-sized capacitors (eight on each side) with the middle terminal held at the common mode of the input signal. There are four unit-sized capacitors on each side for feedback. Two of them are only used for the radix calibration *fi* extraction operation.

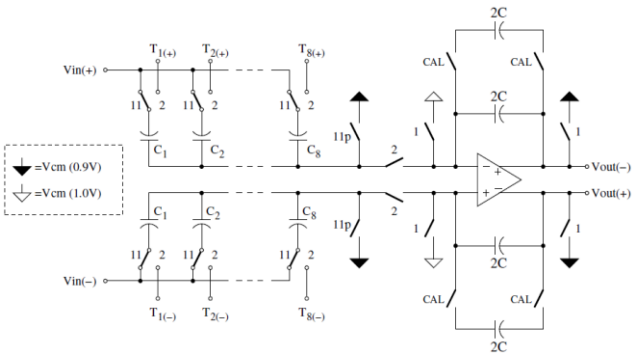

Figure 10. Final MDAC Implementation

The operation of the MDAC is as follows. During the first phase, the input is sampled on the sixteen input capacitors. This phase is also known as the *sampling phase*. The opamp is isolated from the sampling operation, and has its inputs shorted together and outputs shorted together. During this phase, the switched-capacitor common-mode feedback within the main amplifier is also refreshed. The four non-calibration measurement feedback capacitors are also pre-charged to the difference between the input and output common mode of the amplifier; this keeps the input of the amplifier from experiencing a glitch when the MDAC switches to the next phase.

3-4- Comparator

The first stage comparator requires some specialized design to accommodate the special timing needed for continuous-time sampling within the first stage of the Pipeline. Additionally, an offset correction scheme is employed to allow for maximum sample mismatch correction by the digital redundancy of the pipeline architecture.

The comparator circuit is shown in Figure 11. During the first phase (phase 11), the input is sampled on one of the input capacitors while the appropriate reference is sampled on the the other input capacitor. The comparator sampling circuit is matched to the MDAC sampling circuit but is 1/64 the size of the MDAC sampling circuit. Also, during this phase, the inputs of the pre-amplifier are shorted together. The pre-amplifier offset is sampled on the offset storage capacitor at the end of the first phase.

During the second phase (phase 22), the charge stored on the input sampling capacitors is averaged together. This signal is then applied differentially to the inputs of the pre-amplifier and amplified through the offset storage capacitors and applied to the inputs of the differential latch. After a short delay, the latch is allowed to regenerate, and the output value is available to the digital circuits that multiplex and buffer the signals before sending them to the MDAC DAC inputs for the start of the MDAC amplification phase.

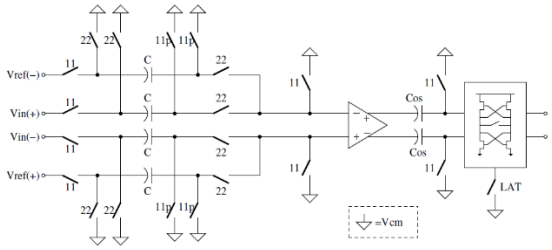

Figure 11. Top-Level Comparator Circuit

Simulation of the comparator verifies its operation. It can resolve 10mV (<0.1 LSB) comparison signals in 4nS (2nS for the pre-amp and 2nS for the latch regeneration).

The pre-amplifier is a simple single-stage amplifier with low current and moderate gain. The common-mode feedback employed is the linear operation MOSFET feedback. Their operation is poor over a wide input range; however, this is of minimal importance as the most important comparator signals are the well-behaved, near-zero-differential signals.

The latch is composed of two cross-coupled positive feedback transistors, current input PMOS transistors and a NMOS reset switch. The reset switch allows the inputs to start near mid-rail and not depend on a race from the supply rail to determine the latched value. This should reduce the effect of device mismatch within the comparator.

The DC current within the latch before regeneration is set by the common mode input provided by the pre-amplifier. This value was chosen to be small (50¹A) so that the total power consumption of the comparator block within the Pipeline ADC would be minimal in comparison to the required bias currents in the MDAC opamp (5mA). The pre-amplifier burns approximately 20¹A. This gives a comparator array power consumption of 1.1mA. The digital portion of the chip begins at the output of the comparator latch and ends at the switch selection circuitry that selects the references to be switched onto the MDAC DAC capacitors during the the amplification phase. There are a few digital circuit blocks needed for correct operation of the ADC. These include latches, bubble correction logic, and digital signal multiplexer.

The Set-Reset Latch is a simple digital circuit that stores digital information within the latch. The S.R. latch is constructed by connecting two cross-coupled NOR gates as shown in Figure 12. The function of this circuit is to drive the output *Q* to a high value whenever the *set* signal is asserted and drive *Q* to a low value whenever the *reset* signal is asserted. Additionally, this signal is held until the opposite signal (set or reset) is asserted again. The operation of the circuit is summarized in Table 4.

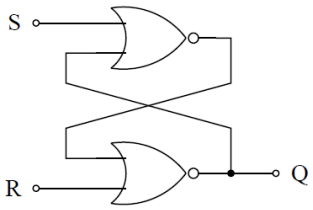

Figure 12. S.R. Latch Circuit

The S.R. latch is used to latch the digital data received by the differential latch at the output of each comparator. The rest stage of the differential latch circuit is such that it looks similar to a logical `00', which keeps the S.R. latch \latched" until the output changes to a `01' or `10'.

3-4-Layout

The layout of the first stage was completed as part of this paper project. There are many layout issues to be considered with the design of a high-resolution ADC. These include signal and reference protection, analog circuit isolation, matching, and clock routing.

The first major concern in poor-planning any mixed-signal circuit is isolation of analog and digital circuits. This is best accomplished by segmenting the design into analog and digital portions and keeping sensitive analog circuits as far away from the digital circuits as possible. Additionally, analog and digital circuits should be on separate power supplies, and each circuit should have a guard ring tied to a low impedance node.

Other major concerns when determining the general layout structure are isolation signal traces themselves. The physical separation of analog and digital blocks will go a long way towards helping this issue, but sometimes it is not possible to keep these signals apart (i.e. switches in the MDAC circuit). When sensitive analog signals must travel near to any other signal, shielding the lines with parallel ground lines (and sometimes top and/or bottom ground planes) is an effective strategy.

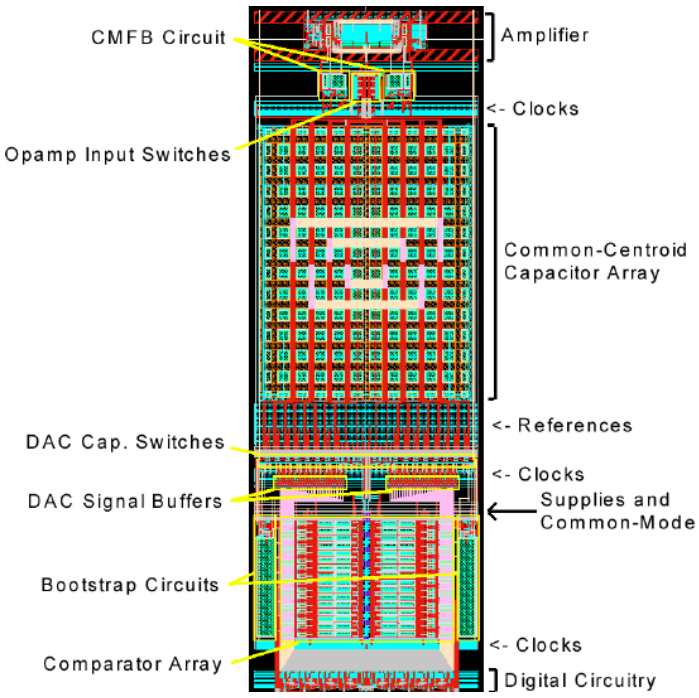

Figure 13. First Stage Layout

The layout for the first stage is shown in Figure 13. Notice that the analog amplifier circuit is on the opposite side as the digital circuitry. Additionally, clock signals only travel horizontally in dedicated clock channels this avoids coupling of the clock signals to signals traversing the height of the stage. The references are grouped and isolated from any potential noise sources. They are also made from wide sheets of metal to improve the response of the node to any transient glitch coupled onto the node.

CONCLUSION

The difficulty of implementing a high-resolution Pipeline ADC in a low-voltage process has been established and explored in detail in this paper. Several solutions to this problem have been explored and an implementation incorporating a few of these solutions has been implemented on the modeling and simulation level. Further development of this design strategy and completion of a test chip are an important next step in the continuation of this work. Some other extensions to this work are as follows:

One other MDAC structure for the rail-to-rail input showed promise and did not require the use of a calibration scheme. A rail-to-rail input Pipeline based on this structure may be a worthwhile exploration. Stage scaling optimization schemes allowing independent changes in stage-resolution and stage-scaling for each pipeline stage may find more optimum configurations for high-resolution Pipeline ADCs. Also better modeling of power consumption of the comparator stages would improve this optimization. Poor capacitor matching (even with common-centroid arrays) may require that some form of capacitor error correction [33, 34] be incorporated into the design.

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